USING THE J-K FLIP-FLOP IN SMALL MODULO COUNTERS*

by Jack Irwin

I. INTRODUCTION

The integrated circuit J-K flip-flop has been touted as a "can saver." The J-K also has an edge over the R-S flip-flop because when both inputs are true (one), it will provide a definable output. Proof of its acceptance is seen in the many IC users who have incorporated its features into their circuit designs. This paper brings together here a number of practical counter circuits that exploit the advantages of the J-K flip-flop.

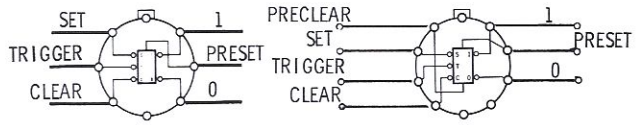
II. J-K OPERATION

A Binary flip-flop must change state with each input (trigger) pulse. Hence, if its state prior to a trigger pulse is true it must go false, and vice versa. Normal operation for a binary R-S flip-flop calls for feedback connections from the outputs to the inputs to control this sequence. By definition,[1,2] a J-K flip-flop does not require the feedback. If we compare the operation of the R-S flip-flop and the J-K flip-flop, Fig. 1, we see that in the fourth condition the J-K flip-flop performs the necessary reversal of states. But in the R-S flip-flop, this condition is not definable—hence, the need for external feedback.

R-S FLIP-FLOP			J-K FLIP-FLOP		
Input t = n		Output t = n + 1	Input t = n		Output t = n + 1
Set	Clear	Q	Set	Clear	Q
0	0	Q^n	0	0	Q^n
1	0	1	1	0	1
0	1	0	0	1	0
1	1	?	1	1	$\overline{Q^n}$

FIG. 1. Gating conditions for R-S and J-K flip-flops compared. "1" is a low (saturation) voltage and "0" is a high voltage.

A typical J-K flip-flop will work as a binary counter stage with its J-K (set and clear) input tied to ground. It will change state upon a trigger input transition from positive to low voltage. For multiple stage counters, connecting the 0 (false) side (see Fig. 2) of the preceding stage to the trigger input will produce "count up" operation for low true logic. Connection to the 1 (true) side will produce "count down" operation. "Count up" is defined as all stages starting false and counting to all true. And "count down" is just the reverse. For positive true logic systems the side of connection would reverse. Figure 3 shows a five stage Mod 32 count-up binary counter using μL 923 elements.



(a) Type 923 (b) Type 926

FIG. 2. Logic diagrams for J-K flip-flops.

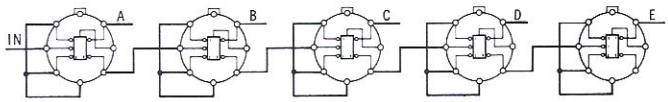


FIG. 3. Five-stage Mod 32 count-up binary ripple counter.

In the ring counter, Fig. 4, a single true state is shifted around the loop. To justify a ring counter, the cost of the additional stages required must be less than that of the gate elements to decode a binary counter and control its count sequence. The ring counter requires one stage per count. Other counters require as few as X stages where 2X is the next highest power of two. As an example, using

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Fig. 4, the Mod 6 counter can be implemented with three stages ($2^3 = 8$). Thus, the cost of the three additional stages must be equal to or less than the cost of six three-input gates. Few instances will occur where the ring counter is economical using integrated circuits.

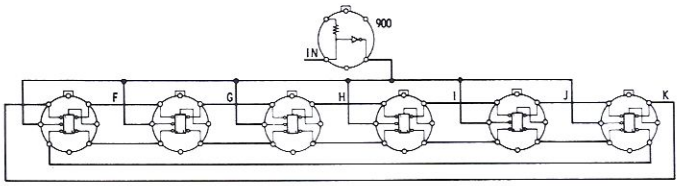
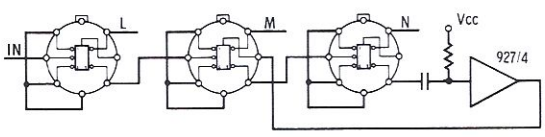


FIG. 4. Mod 6 ring counter uses 6 J-Ks and a driver.

III. PERMUTING TECHNIQUE

Permuting may be used where a pulse is required to feed back and set or reset a stage or group of stages. This technique effectively subtracts the difference in counts between the desired modulo and the next higher power of two. An example, for a Mod 6 counter, is shown in Fig. 5. Although the stage triggers on a transition, the asynchronous (preset) input is a DC input. Therefore, AC coupling must be used for the feedback permuting. While direct connection of a capacitor from the driving stage is possible, it is not recommended due to the differentiation developed. The AC-coupled circuit is identical to the circuits for timing pulses and delays (one shots). In the circuit of Fig. 5, a positive pulse is fed back whose width is equal to the time constant of the capacitor-resistor network.[3]



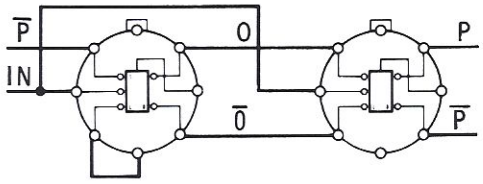
	L	M	N
Q	0	1	0
1	1	1	0
2	0	0	1
3	1	0	1
4	0	1	1
5	1	1	1

FIG. 5. Mod 6 counter with permuting.

Note that with permuting the preset input cannot be directly used for paralleled input or initializing. This draw back may not be as serious with some J-K's as it is with others. Additional factors to be considered include the inherent noise pickup of AC circuits, the space required by the discrete component, and finally, timing margins and variations with environmental conditions.

IV. SIMPLIFYING THE CIRCUIT

Circuit simplification may result from using either the set or the clear (or both) inputs to gate a trigger pulse to set or reset the flip-flop. Thus, trigger pulses may be gated into a stage for a period of time dependent upon the state of one or more other stages. Likewise, one or more input pulses may be inhibited from changing the state of a particular stage. This latter is used on the first stage for odd numbered counts. Likewise the trigger for a stage (N-1) can be used on the next stage (N) if the true term of the first stage is used to gate both the set and clear inputs of the second stage.



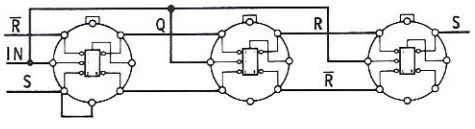
	0	P
0	0	0
1	1	0
2	0	1

FIG. 6. Mod 3 counter uses shift mode binary count.

The Mod 3 counter (Fig. 6) uses a gated shift counter mode to acquire the odd numbered count. Assuming the circuit is in the first state (00), both the set and clear inputs are low due to the zero term at the set input. Therefore, at the low going trigger transition, the first stage changes to the true condition as shown in stage number two (10). The zero of the first stage is shifted into the second stage with no change.

During this state both the set and clear inputs of the first stage are low. Hence, the second trigger input will change the first stage back to its original zero state. The second trigger will shift the one condition of the first stage into the second stage for the third state (01). Because the zero term of the second stage is high during the third state, the trigger will not change the condition of the first stage during the third trigger. The zero condition of the first stage will be transmitted to the second stage. This returns the circuit to its original state (00).

There is a single illegal state that may be encountered when power is applied. Assuming that the circuit starts in this illegal state (11), it will go to the state of 01 upon seeing a trigger pulse. This is a legal state and the circuit will now continue in its prescribed cycle. Note that the conditions are in a binary code even though the circuit is operated in a shift mode. The circuit consists of only the two flip-flop elements.



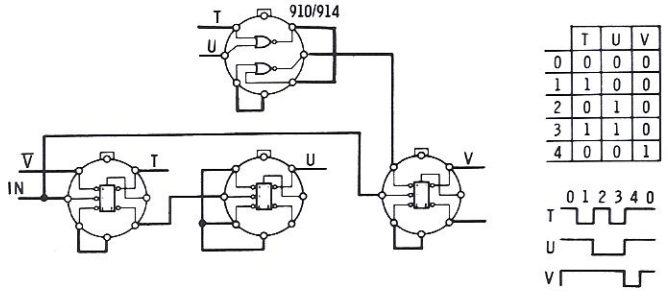
	Q	R	S
0	1	0	0
1	1	1	0
2	1	1	1
3	0	1	1
4	0	0	1

FIG. 7. Minimum-element Mod 5 counter using shift mode.

Figure 7 illustrates a minimum element Mod 5 counter. The count is not in the binary code. It uses a shift mode of operation. The second stage is fed back via the $\overline{R}$ term to the set input of the first stage, Q, to enable the setting of that stage on the fifth count. The true term of the third state, S, is fed into the clear input of the first stage, Q. This shifts a 111 pattern through the circuit each cycle.

V. UPPING THE HARDWARE COUNT

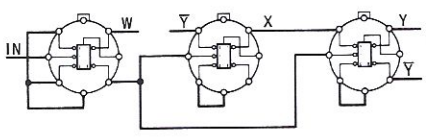
When a Mod 5 counter with binary code is needed the circuit of Fig. 8 is appropriate. The hardware necessarily increases to control the count sequence. The AND function is performed to detect the presence of the fourth state and to set the third stage. Because the output of the AND gate is positive and the J-K requires a low to set it the inverter is needed.[4] One of the dual two-input μL 914 gate elements could be used (instead of the μL 910 element shown) but it would require more loading on the first two stages. The gating could be made up of one-half of a μL 910 (for the AND gate) and one-quarter of a μL 927 quad inverter for the other portion. This would result in usage of three-fourths of an element count if the unused portions could be utilized elsewhere.

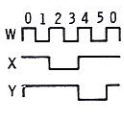


	T	U	V
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1

FIG. 8. Mod 5 counter with binary code.

The Mod 6 counter (Fig. 9) is a minimum circuit since only the three counter stages are needed. From the waveforms (Fig. 9b), it is seen that the first stage, Q, can function as a binary stage. This is the result of having an even modulus. The second stage, X, can function in normal binary except for the sixth count. During the sixth stage (101), a condition must be used to inhibit the setting of the stage. The third stage, Y, may be used for this signal. Even though the third stage, Y, is low during the fifth state (001), the trigger input from the zero side of W to the second stage X is going high and will not trigger X.





	W	X	Y
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1

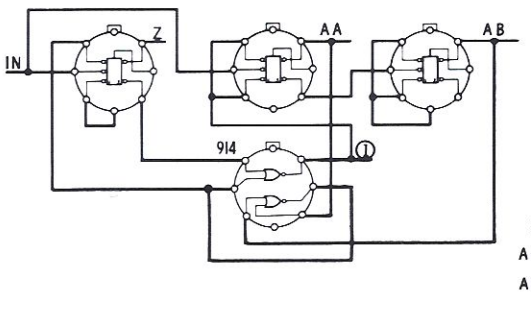
a. b.

FIG. 9. Mod 6 counter with binary code.

The waveform for the third stage dictates the inputs to the stage. The only signal available to change the stage at the necessary times is the zero term of W. With X on the set input, the third stage will change state (set) at the fourth count with both the set and clear input low. During the sixth count, the low clear input will reset the stage to zero, returning the circuit to the first state (000).

VI. BC COUNTER USES SET INHIBIT

The Mod 7 counter of Fig. 10 works in binary code. The first stage has a set inhibit during the seventh count. The second stage will change state when either the first stage is true or when the seventh count is recognized due to the gating. The third stage is connected as a normal binary stage. The required gating would be a μL 914 element. The true terms of the second and third stages AA and AB are ANDed by the one gate. The resulting positive output during the seventh state inhibits the first stage and is used in the second gate to OR with the first stage to enable the second stage to change state.



	Z	AA	AB
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1

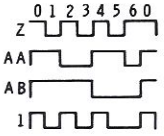
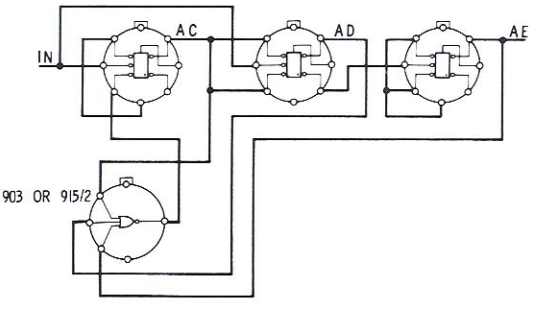


FIG. 10. Mod 7 counter with binary code.

The Mod 7 counter of Fig. 11 is similar to that of Fig. 10. It could be constructed with one-half of a μL 915 element in addition to the necessary three J-K's. In this circuit the seventh count is detected and used only to inhibit the clearing of the first stage.



	AC	AD	AE
0	1	0	0
1	0	1	0
2	1	1	0
3	0	0	1
4	1	0	1
5	0	1	1
6	1	1	1

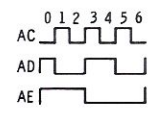
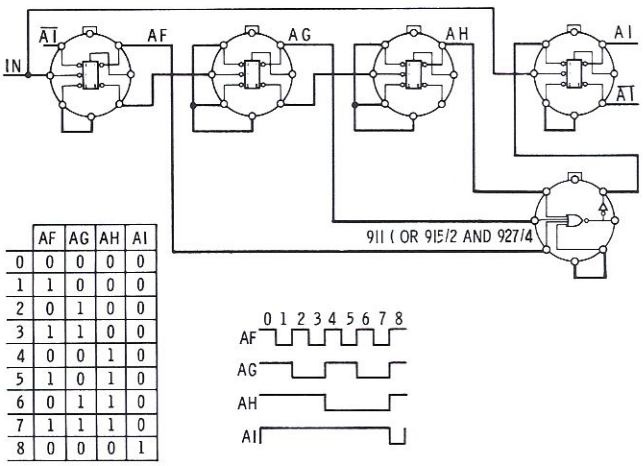


FIG. 11. Mod 7 counter with binary code (uses ½ less element than Fig. 10).

Cost and Hardware Implications

The J-K flip-flop avoids the extra circuitry needed with conventional flip-flops to provide the necessary logical conditions for a memory stage, and in many cases it permits the use of fewer cans. In some cases power supply requirements are reduced (a J-K flip-flop replacing a pair of Micrologic shift registers might dissipate only half the power). Frequently only part of an element is required to perform a gating function, leading to the possibility of the other portions being used elsewhere. Lower modulo counters can be combined to provide larger counts. In certain systems, this means that circuits may be packaged as subassemblies. The result can be repeated usage of common blocks and reduced costs of PC boards, assembly, and checkout. The μL 923 flip-flop is shown in all diagrams, yet the μL 926 (Fig. 2) or other J-K flip-flops could be used (the exact pin connections, circuit configurations, and signal levels might vary). The μL 926, for example, with its buffered outputs, would be applicable where additional drive is needed (say for decoding).

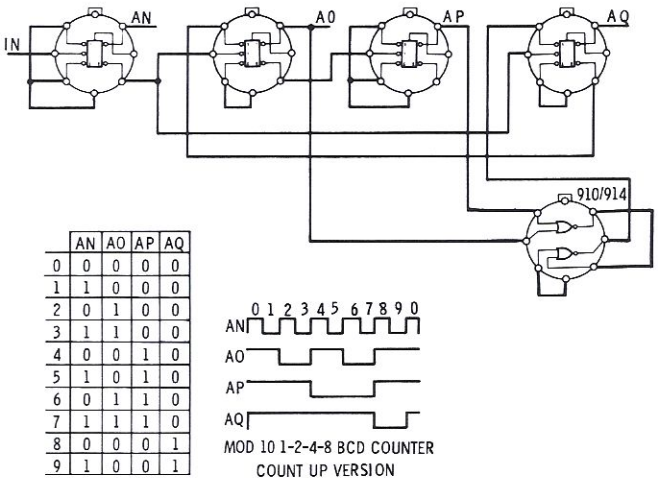
The Mod 9 circuit of Fig. 12 required only one additional element to perform the desired sequence in binary code. The μL 911 element is used for the AND function necessary to set the fourth stage, J. The fourth stage inhibits the setting of the first stage during the ninth count. With the μL 915 and μL 927 elements, the gating requires only 3/4 of an element (but it loads the first three stages more).



	AF	AG	AH	AI
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1

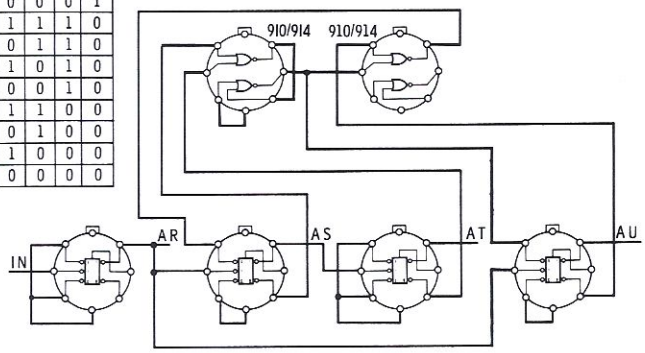
FIG. 12. Mod 9 counter with binary code.

One of the most commonly used counter circuits (the 1-2-4-8 BCD) is shown in Fig. 13. The gating detects the presence of the eighth state and enables the setting of the fourth stage (AQ). The fourth stage is fed back to inhibit the setting of the second stage (AQ to the set pin of the AO stage). The gating could be made up from various combinations of gates. Probably the most common is one μL 910 element. Shown in Fig. 14 is the count down version of this circuit. This is a popular count sequence. It does, however, require more gating.



	AN	AO	AP	AQ
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

FIG. 13. Mod 10 1-2-4-8 BCD counter (count-up version).



	AR	AS	AT	AU
9	1	0	0	1
8	0	0	0	1
7	1	1	1	0
6	0	1	1	0
5	1	0	1	0
4	0	0	1	0
3	1	1	0	0
2	0	1	0	0
1	1	0	0	0
0	0	0	0	0

FIG. 14. Mod 10 1-2-4-8 BCD (count-down version).

VII. EASY DECODING BALANCES COST OF J-K

The main advantages of the "two by five" version of the Mod 10 counter (Fig. 15a) is that of ease in decoding. A two input gate is necessary and sufficient to decode any one of its stages. In light of this, the cost of the additional J-K may be outweighed. The circuit has a further advantage in that it is a synchonous counter: that is, all outputs change at the clock time rather than being delayed by preceding stages changing state.

Computerese: A "Quickie" Review

Modulo (or Mod): Applied to a counter circuit indicates the number of input pulses required before the count cycle is repeated. Thus, a modulo 10 counter will accept 10 pulses and then repeat the steps. The counter must have a discrete, unique state for each of these counts. A binary counter stage or binary flip-flop, with its two states, counts in Mod 2. Two binary counters connected such that the second is triggered upon completion of the cycle of the first counts in Mod 4. There are four states for the latter: (1) both (stages) false, (2) the first true and the second false, (3) the first false and the second true, and (4) both true.

Permuting: The use of feedback to force some state in a counter at a prescribed time.

J-K Flip-flop: The J-K flip-flop, like the R-S flip-flop, has these characteristics: (a) if both inputs (R and S or J and K) are zero, the memory element will not change state; (b) if the set (S or J) input is true and the reset (R or K) input is false, it will go to the "1" state; (c) if the reset input is true and the set input is false, it will go to the "0" state. However, if both inputs are true, the R-S flip-flop will not go into a definable state, whereas the J-K flip-flop will reverse state. (See the truth table, Fig. 1.)

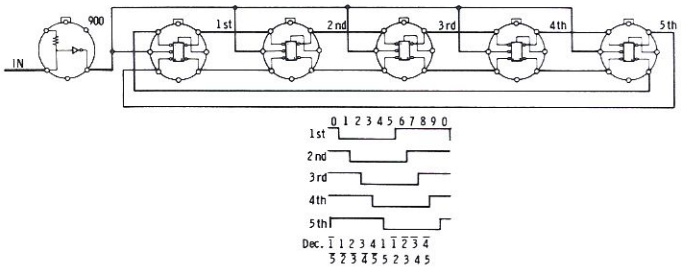


FIG. 15a. Mod 10 shift counter.

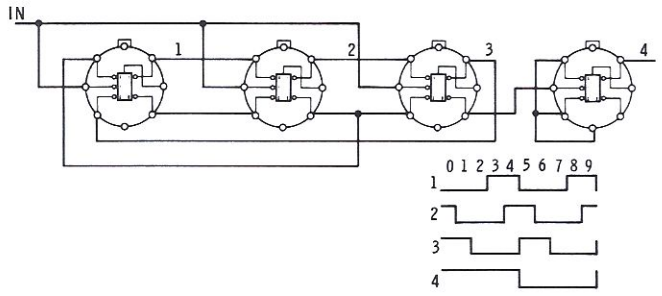


FIG. 15b. Mod 10 counter combines Mod 5 and Mod 2.

The bi-quinary circuit of Fig. 15b is best in those systems using a display or counting technique working in this mode. It is particularly useful when working with certain display tubes. The advantages of the particular Mod 5 is the requirement of only two-input gates to decode the five states.

When a Mod 10 counter is needed for frequency division, the circuit of Fig. 16 is desirable since it only uses the four

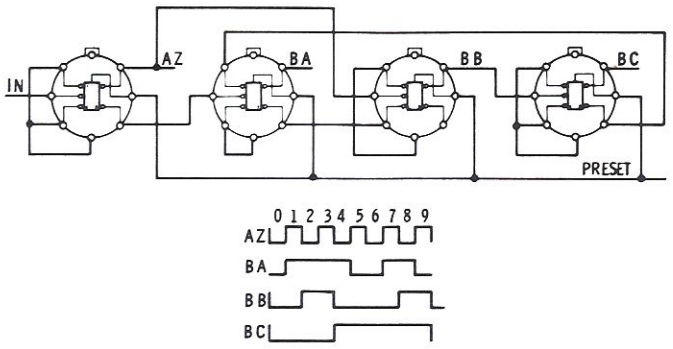
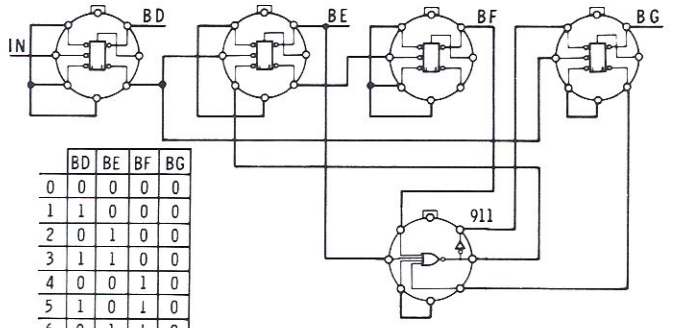


FIG. 16. Minimum-element Mod 10 counter.

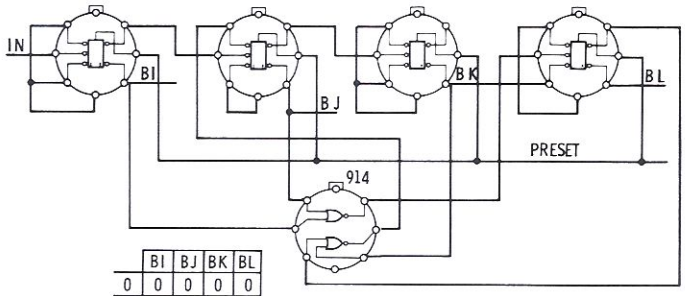
binaries without additional gating. It has the disadvantage that it is not in a weighted code and therefore is more useful in the mentioned application. It could be decoded into its ten states for ten-line output.



	BD	BE	BF	BG
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

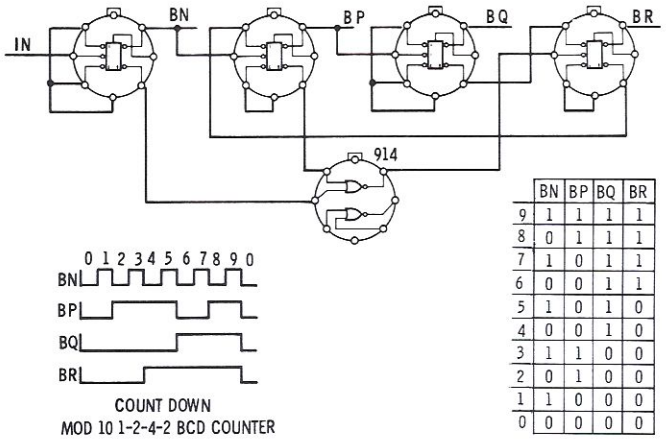
FIG. 17. Mod 10 counter in 1-2-4-2 BCD code.

Another commonly used code is the 1-2-4-2 BCD code. Figures 17 and 18 illustrate two versions of this circuit differing only in the element used for the gating. Figure 19 is another version for count down operation. It needs but one-half of a μL 914 element for the gating.



	BI	BJ	BK	BL
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	1	1	1
9	1	1	1	1

FIG. 18. Mod 10 counter in 1-2-4-2 BCD code with alternate gating.

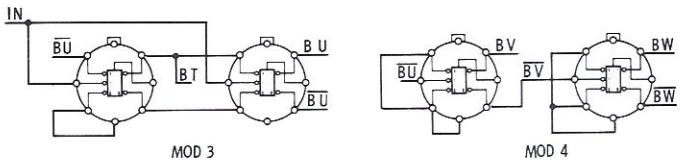


	BN	BP	BQ	BR
9	1	1	1	1
8	0	1	1	1
7	1	0	1	1
6	0	0	1	1
5	1	0	1	0
4	0	0	1	0
3	1	1	0	0
2	0	1	0	0
1	1	0	0	0
0	0	0	0	0

FIG. 19. Mod 10 counter in 1-2-4-2 BCD code (count-down version).

VIII. DESIGNING HIGHER MODULO COUNTERS

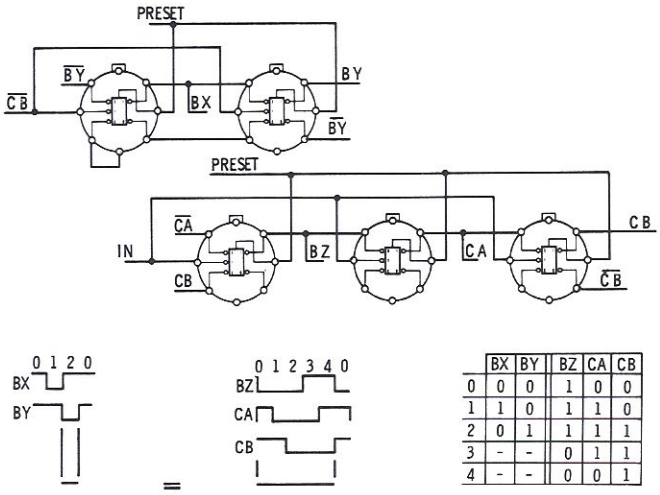
For higher modulos the techniques outlined here can also be utilized. As an example, the Mod 11 or Mod 13 counter could use the same method as the Mod 9 counter or possibly the Mod 5 counter of Fig. 7 with the increase of a stage. In the latter case, a more complex waveform would be needed because a normal or shift type counter has a maximum count of 2 x N, where N equals the number of stages. This makes higher count shift registers unfeasible because the binary counter has a maximum of 2^N counts. Normally gating hardware is required for the more complex shifted waveforms. This might result in a more costly circuit than the binary version.



	BV	BW	BT	BU
0	0	0	0	0
1	1	0	1	0
2	0	1	0	1
3	1	1	-	-
	MOD 4		MOD 3	

FIG. 20. Mod 12 counter can be made using Mod 4 (top) and Mod 3 (bottom) counters.

A technique that has merit for larger counts that are even, or products of the lower modulo counters shown above, is to use combinations of these circuits in series. Thus, a Mod 12 counter may be made up of a Mod 4 counter and a Mod 3 is shown in Fig. 20. The sequence is reversible; that is, the Mod 3 may be before or after the Mod 4. The Mod 12 counter may also be made up using a Mod 2 and a Mod 6 counter.



	BX	BY	BZ	CA	CB
0	0	0	1	0	0
1	1	0	1	1	0
2	0	1	1	1	1
3	-	-	0	1	1
4	-	-	0	0	1

FIG. 21. Mod 15 counter.

Using this method for a Mod 15 counter (Fig. 21), no gating element is required using the Mod 3 counter and the Mod 5 counter of Fig. 7. It does require a fifth J-K, but the decoding may be simpler. The Mod 10 counter of Fig. 15b shows the Mod 5 of Fig. 7 combined with a basic Mod 2.

IX. REFERENCES

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